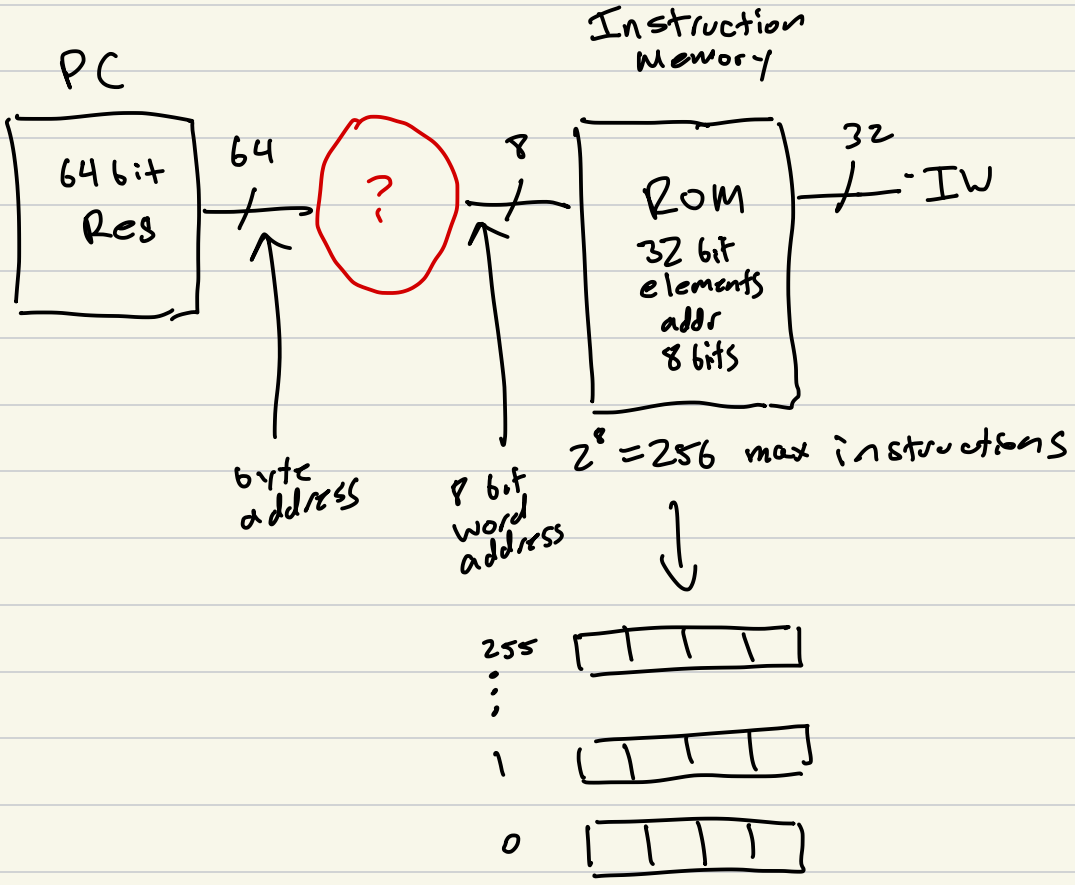
# CS315-01 Processor Design Decoding

## Lab 05 - RegFile and ALU

PC byte address → word address

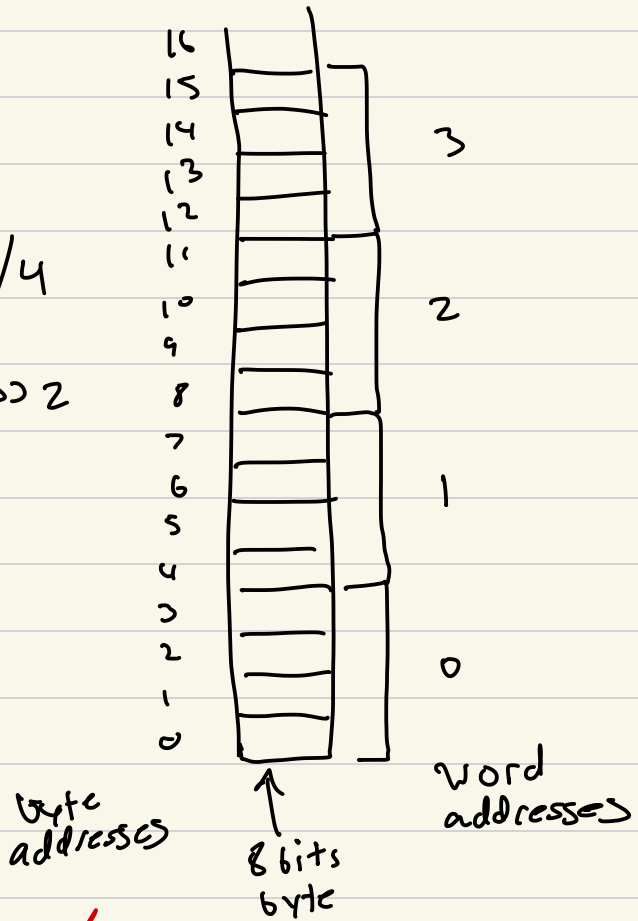


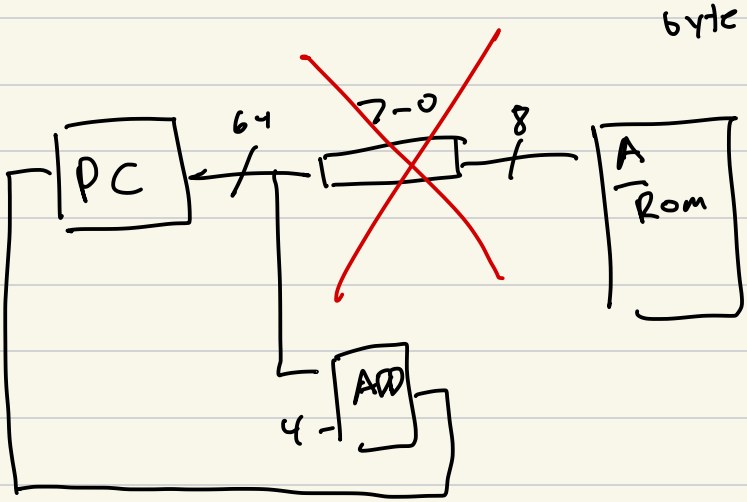
# Memory

addr_byte

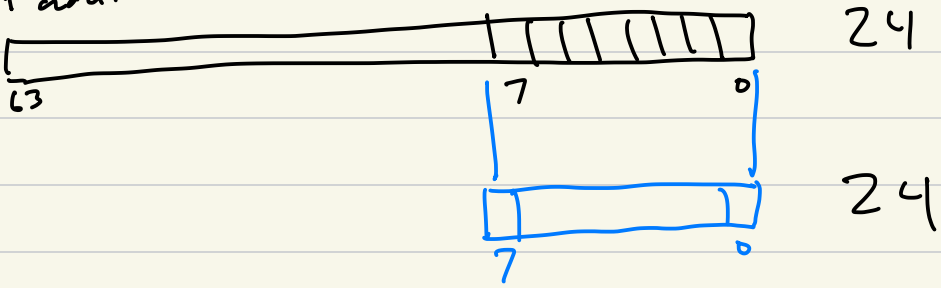
addr_word = addr_byte / 4

addr_word = addr_byte >> 2



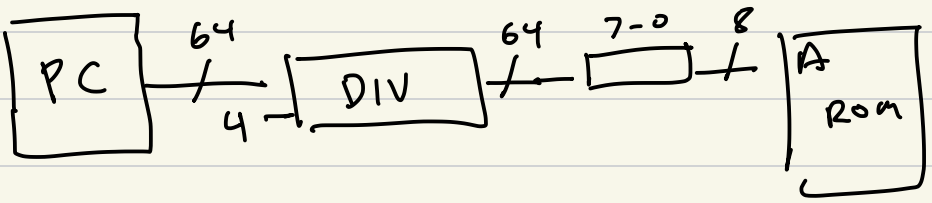
64 bit addr



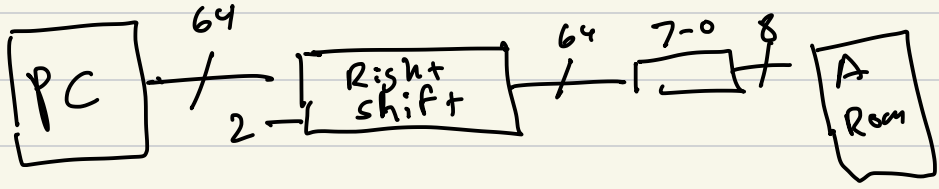

24

24

① PC → 64 → DIV (4) → 64 → 7-0 → 8 → A Rom




② PC → 64 → Right shift (2) → 64 → 7-0 → 8 → A Rom

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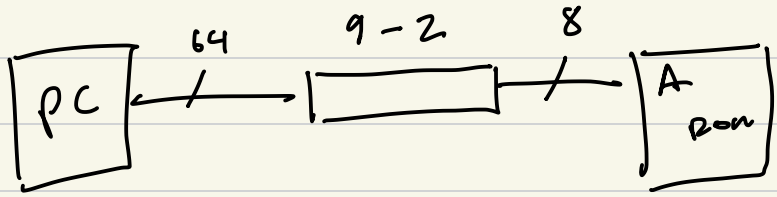
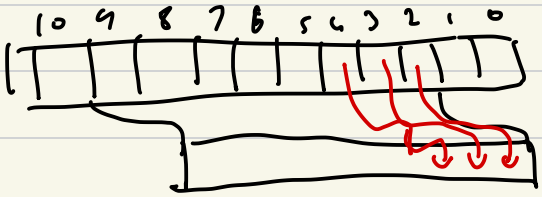
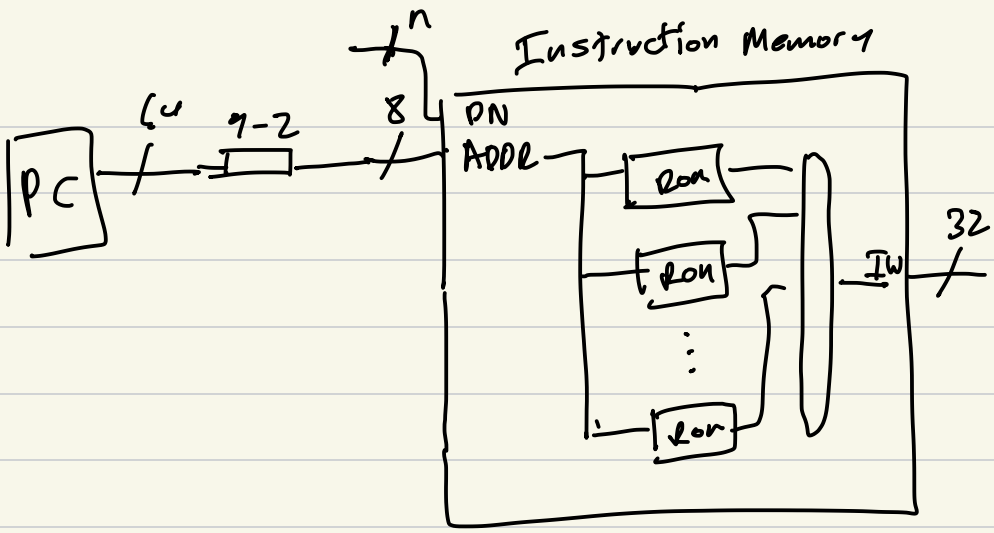
③ PC → 64 → 9-2 → 8 → A Rom



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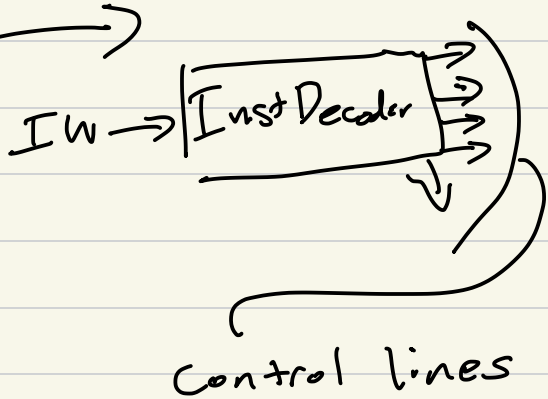
Decoding

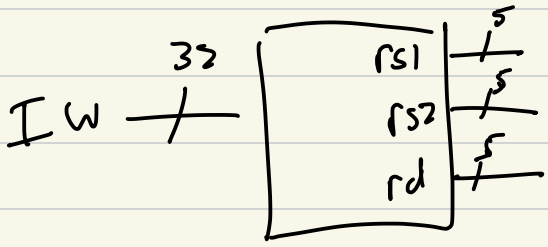
Reg Decoder → get reg #s

Imm Decoder → form 64 bit signed immediates

Inst Decoder →



# Reg Decoder

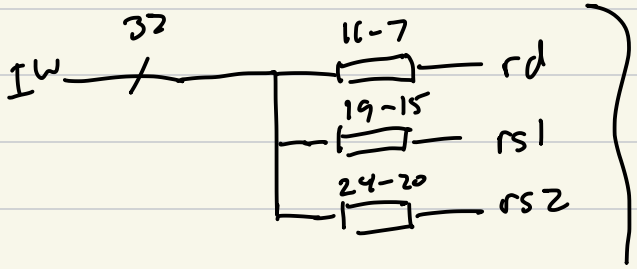



⇒ RegFile

add to, t1, t2

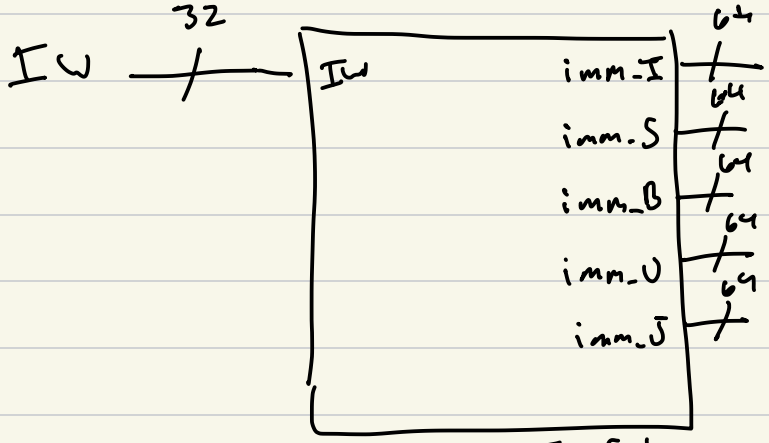
WR RR0 RR1

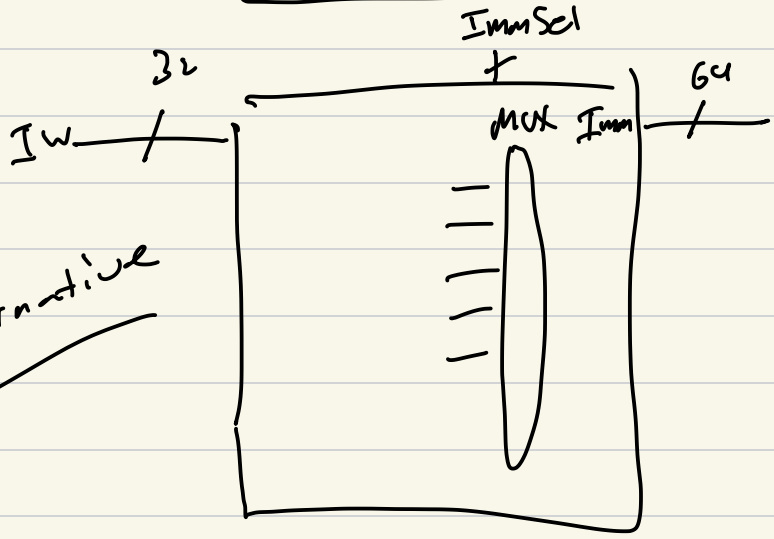
one splitter




Can change order in splitter config

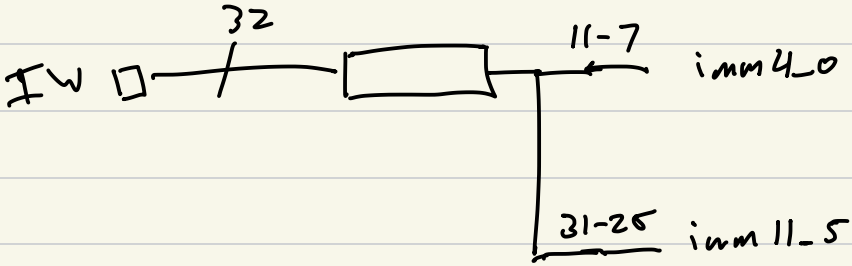
# Imm Decoder



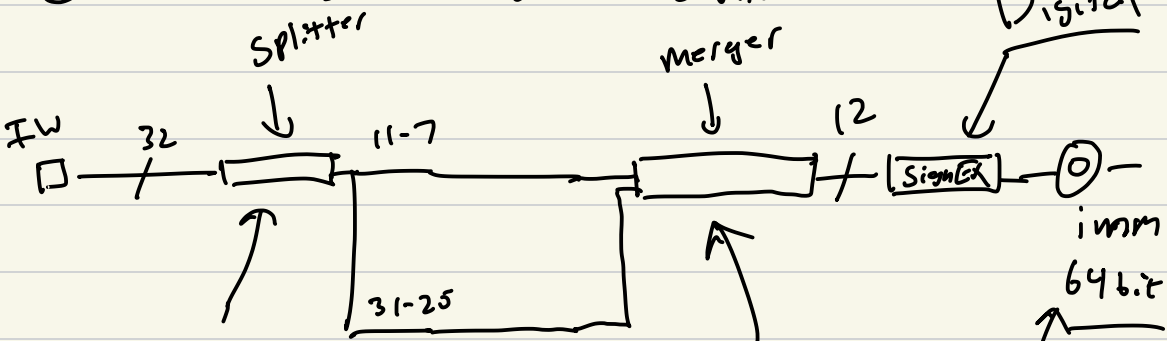




Good Alternative

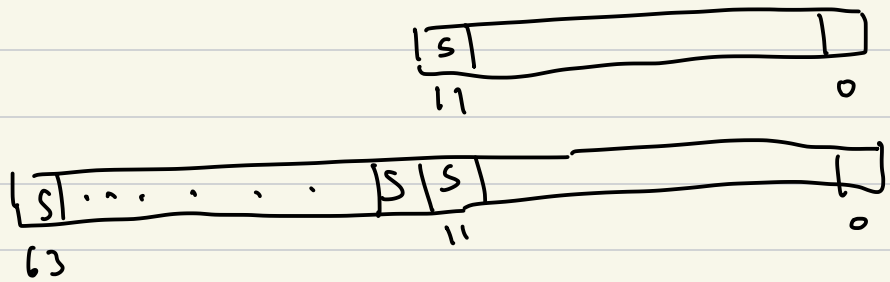
# S-Type Immediate



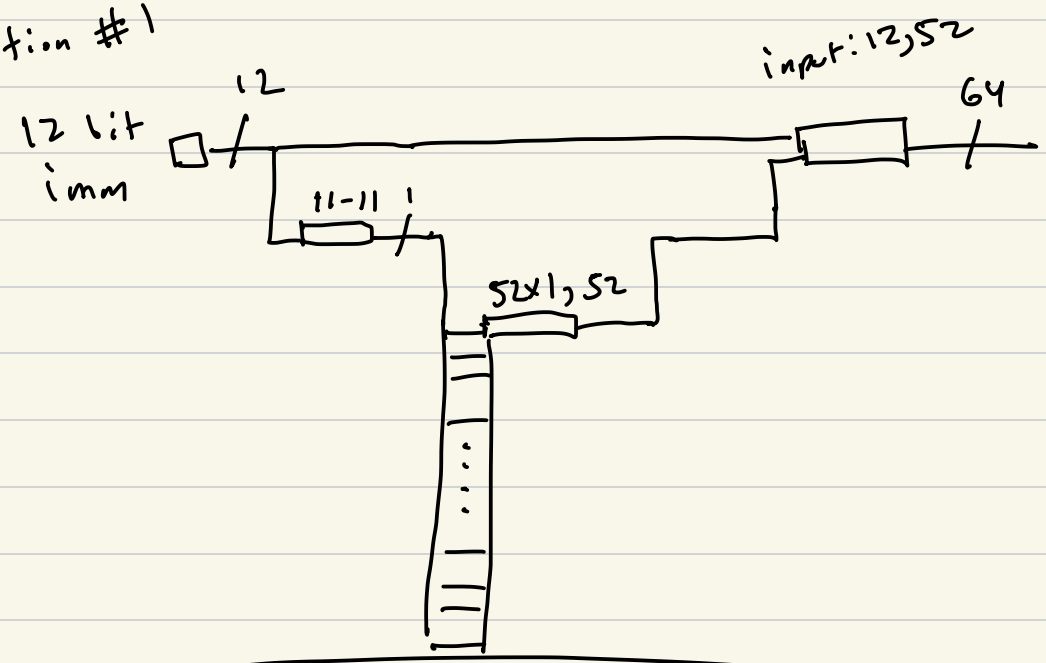

Goal: To Construct a 64 bit Signed value



# How to implement the sign extender




Option #1




Option #2